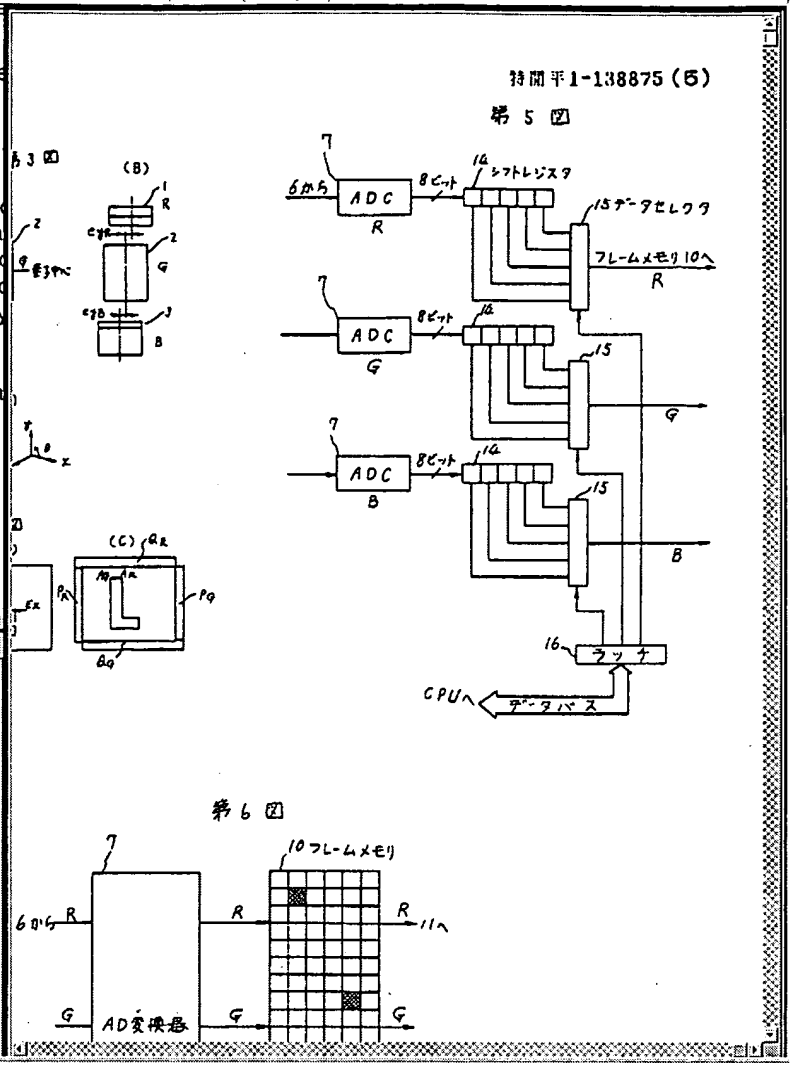
adjusting the timewise relation of output signals of plural image pickup elements resolving a light from an object into object image of plural color components and applying photoelectric conversion to each color compone image.

CONSTITUTION: Each color signal subject to AD conversion 7 is given 8-bit shift register 14 and a data selector 15 and delayed relatively by a predetermined time through measurement in advance. The delay time is by preserving the data from a CPU into a latch 16, the function of the data selector 15 is used according to the data and the color density data is read from the position shifted by the required shift and given to the frame memo 10. The delay circuit and the delay time controller are provided in this way to attain the alignment of the position for plural solid-state image pickup elements in terms of electric circuit, then the mechanical positioning requesting the accuracy in micro-order is facilitated for color mis-alignment correction.

	U	1	Document ID	Issue Date	
1			JP 01138875 A	19890531	COLOR
2			US 6061091 A	20000509	Detection acquisitio
3			US 4640613 A	19870203	Image da



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Brief Summary Text - BSTX (20):

As an example of a particular system, consider a digital image acquisition device such as a digital camera. The imaging sensors may form an array of 1200 elements by 1000 elements, for a total of 1.2 million sensors. To form a digital image, an output from each sensor must be converted to a corresponding digital number value. In order to allow timely re-use of the imaging array, all 1.2 million conversions should be carried out quickly, perhaps necessitating a single very fast A/D converter or a set of slower A/D converters operating in parallel. It may be desired that the imaging array and processing circuitry be on a single small chip so that the camera is physically very small and can be cheaply manufactured. However, the design may also require long operation time with a low-capacity battery as a power supply.

Detailed Description Text - DETX (15):

Prior art SA converters can have relatively compact implementations. FIG. 2 shows a block diagram of an 8-bit SA A/D converter taken from page 623 of the second edition of THE ART OF ELECTRONICS. The principal components are a first comparator 10, an 8-bit D/A converter 22, a successive approximation register 24, an 8-bit latch and output drivers 26, and successive approximation control logic 28.

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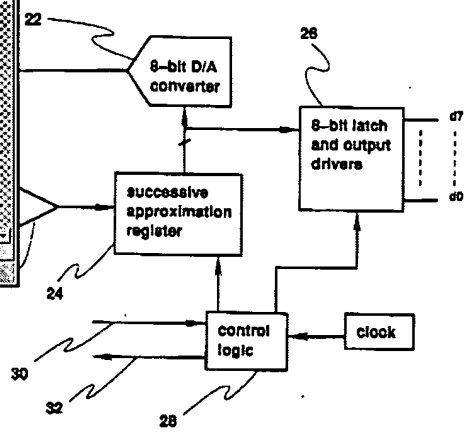
	U	1	Document ID	Issue Date	
15			US 5809270 A	19980915	Inverse q
16			US 6611222 B1	20030826	Low-com
17			US 5101270 A	19920331	Method a correlatio

FIG. 2



Claims Text - CLTX (1):

1. An imaging system comprising: a semiconductor substrate; a plurality of photosensitive pixels, located within said semiconductor substrate, each of said photosensitive pixels sensitive to a specified color of light and said plurality of photosensitive pixels collectively sensitive to at least three different primary colors of light; an A/D conversion element, located in said substrate, and configured to produce digital values from at least a plurality of said photosensitive pixels; an interpolator element, located within said semiconductor substrate, and receiving said digital values from said semiconductor substrate, and receiving said digital values from said A/D conversion element, said interpolator element including a register which stores bits of said digital values, and interpolates among said bits of said digital values to interpolate a level of a spectral component for one of said primary color pixels based on a received level of another primary color pixel.

Claims Text - CLTX (3):

3. An imaging system as in claim 1, herein said photosensitive pixels includes CMOS image sensing pixels.

	U		Document ID	Issue Date	
25			US 6708124 B2	20040316	Impulsive
26			US 6704049 B1	20040309	Interpolat
27			US 6304243 B1	20011016	Light valv

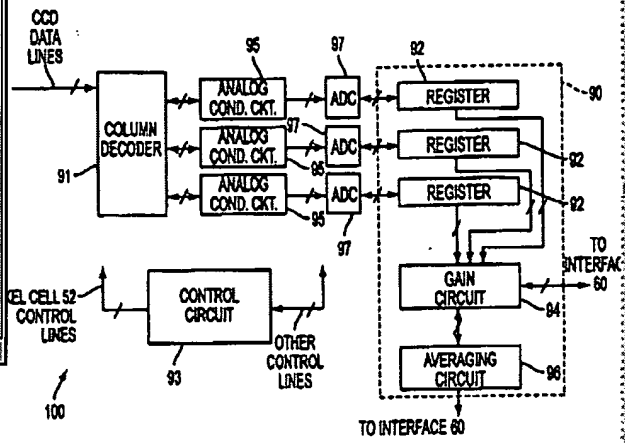


FIG. 8

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File Edit View Tools Window Help

——— KWIC ———

Detailed Description Text - DETX (12):

The incident light focused on the light receiving surface of the CCD line image sensor is photoelectrically converted into an image signal V.sub.CCD for each pixel by the CCD line image sensor. The analog voltages of the image signal V.sub.CCD are serially transmitted to one analog register. The analog voltage in that register is digitised by a 12-bit A/D-convertor (Analog to Digital Convertor or ADC). The bit depth of the image sensor is thus 12 bit. For colour images this results in 36 bits per pixel. If the 12 bits are reduced to 8 bits in a later stage, 24-bit colour images are generated. The analog voltage applied at the input of the ADC is minimal if the intensity or illuminance I (for a fixed exposure time) of the corresponding photo-sensitive element was below a certain lower limit. In such case, it is usual to deliver a digital value of 0 at the output of the ADC. If the intensity I reaches a specific upper limit (again for a fixed exposure time), then the analog voltage applied to the input of the ADC reaches a maximal value, for which the ADC is said to go in saturation. In such case, the ADC traditionally outputs its maximum digital value I.sub.MAX. For a 12-bit ADC, this maximum digital value I.sub.MAX may be 4095. Since the digital values output by the ADC correspond

Details | Text | Image | HTML | KWIC

	U	1	Document ID	Issue Date	
1	☐	☑	JP 01138875 A	19890531	COLOR
2	☐	☐	US 6061091 A	20000509	Detection acquisitio
3			US 4640613 A	19870203	Image da

US006061091A

s Patent [19]

[11] Patent Number: 6,061,091

[45] Date of Patent: May 9, 2000

AND CORRECTION FOR
LECTIONS IN DIGITAL
TION

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em; Nick Geybels, Wilrijk, all
um

vaert N.V., Mortsel

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1997

Application Data
No. 60/025,121, Aug. 30, 1996.

cation Priority Data

ropean Pat. Off. 96201303

...... H04N 5/217; H04N 5/202; H04N 5/238

...... 348/241; 348/254; 348/364; 358/522; 382/170; 382/171

.... 378/98.7, 98.8,
11; 358/522; 348/254, 364, 241; 382/170, 171

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0 335 419 10/1989 European Pat. Off. .
0 691 627 1/1996 European Pat. Off. .
WO 92/05509 4/1992 WIPO .

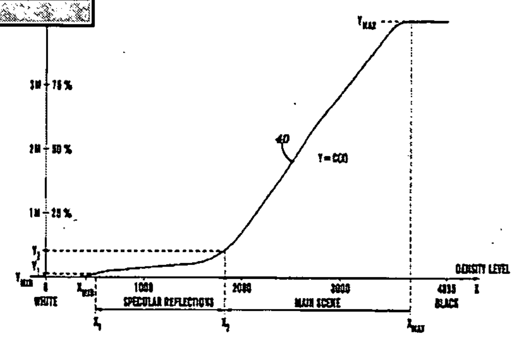
Primary Examiner—Wendy Garber
Assistant Examiner—Eric Ferguson
Attorney, Agent, or Firm—Robert A. Sabourin; Edward L. Kelley

[57] ABSTRACT

Image processing parameters for gradation correction of a digital image from a scene, which includes specular reflections may be seriously influenced by the presence of those specular reflections. Therefore, a method is developed to detect the presence of specular reflections in a scene, to modify the exposure time of the photo-sensitive means, which converts a luminous image to electronic image signals and to apply a gradation correction to the image data thus acquired. In one embodiment a digital camera is used to capture the image data, a cumulative histogram is built and two characteristic cumulative frequencies are used to determine via the histogram specular densities and highlight densities. The relative position of these density values indicates whether specular reflections are present, and give suitable parameters for setting an optimal exposure time and for computing a gradation correction curve.

18 Claims, 4 Drawing Sheets

VE FREQUENCY OF DENSITY



Detailed Description Text - DETX (41):

The bit cells in the ADC 64 are scanned from MSB to LSB by a shift register type scanner in the bit cells. A dynamic design of the shift register is used, which requires two clocks to control the progress of the scan and one triggering signal to start the scan. One bit cell in the scanner has two clock converters and one NOR gate. FIG. 14 shows the design of the shift register and FIG. 15 is a flowchart explaining its operation. ST is the starting trigger pulse that loads a one into the shift register; S1 corresponds to BS1 in FIG. 9; and S2 corresponds to BS2 in FIG. 9. After the shift register is started, the rising edge of CK1 makes the first bit cell selected by an output high at that cell address and the following rising edge of CK2 deselects the cell by making the output low again. The next clock cycle does the same operation to the second bit cell and so on. The output of the shift register selects which bit of the capacitor bank is selected. The size (aspect ratio) of the NMOS transistors is 10/2, and that of PMOS transistors is 20/2.

Detailed Description Text - DETX (63):

Both the ADCs 64, 92 have been constructed and shown to be functional. The ADCs were laid out using 2 micron design rules, fitting in a 40 micron width. The length of the single-sided ADC 64 was 4 mm and the double-sided ADC 92 was 6 mm. The double-sided ADC was suitable for a column-parallel ADC architecture

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	U	1	Document ID	Issue Date	
6			US 5218442 A	19930608	Camera v
7			US 5880691 A	19990309	Capacitiv analog-to
8			JP 01138875 A	19890531	COLOR

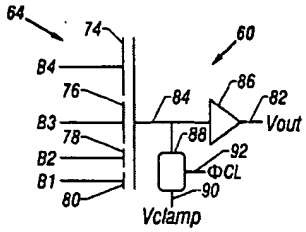


FIG. 7

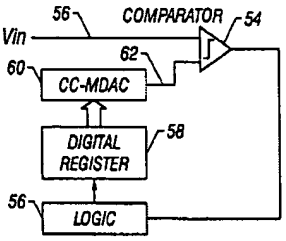


FIG. 8

Detailed Description Text - DETX (4):

The output signals from the light sensors may be supplied in series or parallel transmission to the ADCs. For the purpose of shortening the measurement time, however, parallel transmission of the output signals is preferred. The ADCs 300L and 300R convert the analog signals from the light sensors into digital values each having 1 bit, or a desired number of bits, which are then stored in associated registers 400L and 400R. These registers may comprise shift registers having as many stages as there are sensors in the respective light sensor arrays 100L and 100R. The shift registers 400L and 400R store the quantized digital values in the same sequence as the spatial sequence of the luminous intensities of the images falling on the light sensor arrays. Where the output signals from the ADCs are of multiple bits, the shift registers are composed of as many binary shift registers as there are the signal bits. The image data items are stored in the shift registers 400L and 400R at digital value distributions or shift register stages which are shifted by the deviation distance x between the left and right images on the light sensor arrays 100L and 100R.

Detailed Description Text - DETX (27):

The time required for quantizing analog image signals from the light sensors

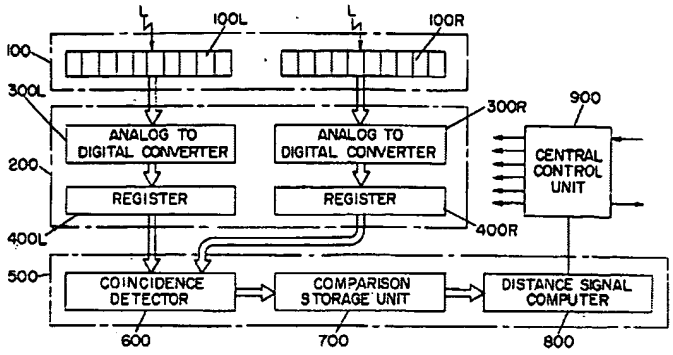
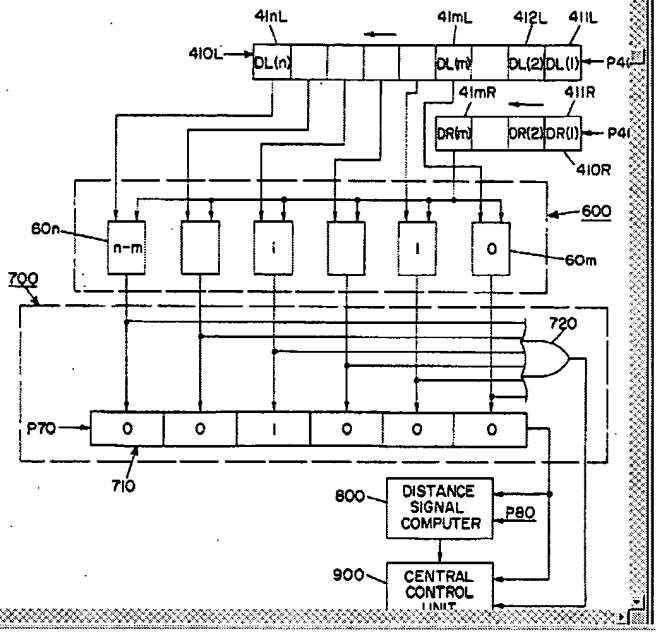


FIG. 4



	U	1	Document ID	Issue Date	
16			US 4292684 A	19810929	Format fc
17			US 4640613 A	19870203	Image da
18			US 4539279 A	19850903	Image de

intervals, and counting during said second sampling interval to cause said time varying reference signal to nonlinearly ramp from said maximum level to a second level during the second sampling interval, said second level being lower than said first level.

Claims Text - CLTX (43):

17. The image sensor of claim 15, wherein each said comparator provides a logic level output to an associated one of said up/down counters, and each up/down counter being responsive to a predetermined state of said logic level output to stop counting.

Claims Text - CLTX (50):

19. The A/D converter of claim 18, further comprising an n-bit shift register for shifting out the n-bit code of said successive approximation register once the least significant digit is resolved.

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	U	1	Document ID	Issue Date	
21	☐	☐	EP 1107581 A	20010613	Image rec is connec store inst
22	☐	☑	US 5920274 A	19990706	Image se
23			US 4553167 A	19851112	Image sig

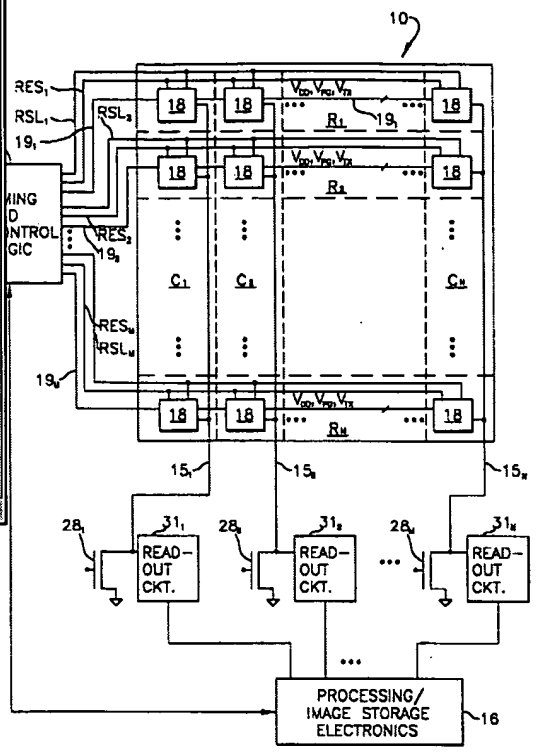


FIG. 2 (PRIOR ART)

and any other type of image sensor can be used.

Detailed Description Text - DETX (71):

Then, as shown in FIG. 12(A) four pulses .phi.HA serially transfer the content of the register 107 from the output terminal 1015 so as to complete the reading of the content of the register 107. An A/D converter 1121 converts the signal from the output terminal into a digital signal. The signal of each bit of the register 107 is, for example, converted into four bit information by the A/D converter. On the other hand, during the time the pulses .phi.HA are delivered, as shown in FIG. 12(A), 16 pulses .phi.HD' are delivered such that as mentioned the A/D converted signal of each bit of the register 107 is applied to the input terminal 1010 via the switch 1118 and transferred to the register 108. Thus, the light signal of the first bit 71b of the register 107, namely, the light signal stored in the picture element [41] is independently transferred to the bits 1b-4b of the register 108 bit by bit as a four bit digital value. In the same way the light signal stored in the picture element [42] is transferred to the bits 5b-8b of the register 108 as a four bit digital value, that stored in the picture element [43] to the bits 9b-12b of the register 108 and that stored in the picture element [44] to the bits 13b-16b of the register 108.

FIG.10

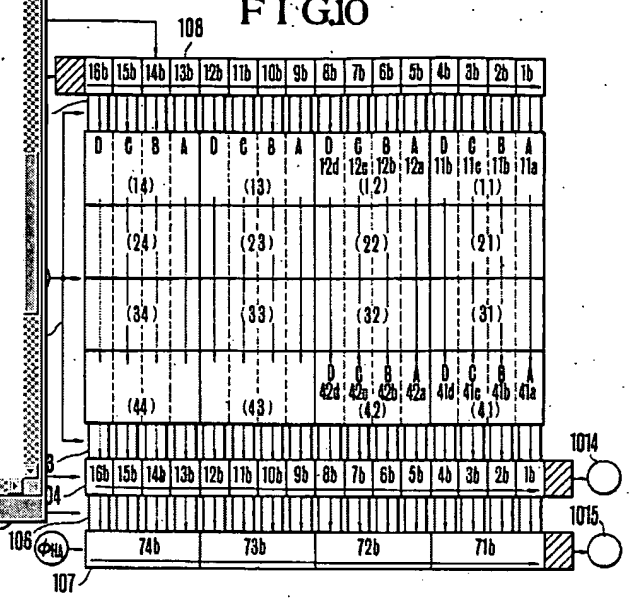
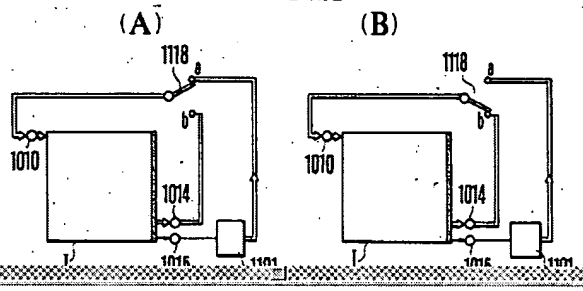


FIG.11



	U	1	Document ID	Issue Date	
22			US 5920274 A	19990706	Image se
23			US 4553167 A	19851112	Image sig
24			US 4833724 A	19890523	Imaging d

Detailed Description Paragraph Table - DETL (145):

TABLE B.3.4 Table 2: Huffman ALU microinstruction fields Field Value Description Bits OUTSRC RSA6 run, sign, A register as 6 bits 0000 (specifies ZZA zero, zero, A register 0001 sources for ZZA8 zero, zero, A register Is 8 bits 0010 run, sign and ZZADDU4 zero, zero, adder o/p ms 4 bits 0011 level output) ZINPUT zero, input data 0100 RSSGX run, sign, sign extend o/p 0111 RSADD run, sign, adder o/p 1000 RZADD run, zero, adder o/p 1001 RIZADD input run, zero, adder output ZSADD zero, sign, adder o/p 1010 ZZADD zero, zero, adder o/p 1011 NONE no valid output - out_valid set to zero 11XX REGADDR 00 - 7F register file address for ALU access 7 bits REGSRC ADD drive adder o/p onto register file i/p 0 SGX drive sign extend o/p onto register file i/p 1 REGMODE READ read from register file 0 WRITE write to register file 1 CNGDET TEST update change detect if REGMODE is 0 WRITE (change HOLD do not update change detect bit 1 detect) CLEAR reset change detect if REGMODE is READ 0 RUNSRC RUNIN drive run i/p onto run register i/p 0 (run source) ADD drive adder o/p onto run register i/p 1 RUNMODE LOAD update run register 0 HOLD do not update run register 1 ASRC ADD drive adder o/p onto A register i/p 00 (A register INPUT drive input data onto A register i/p 01 source) SGX drive sign extend o/p onto A register i/p 10 REG drive register file o/p onto A register i/p 11 AMODE LOAD update A register 0 HOLD do not update A register 1 SGXMODE NORMAL sign extend with sign 00 (sign extend INVERSE sign extend with

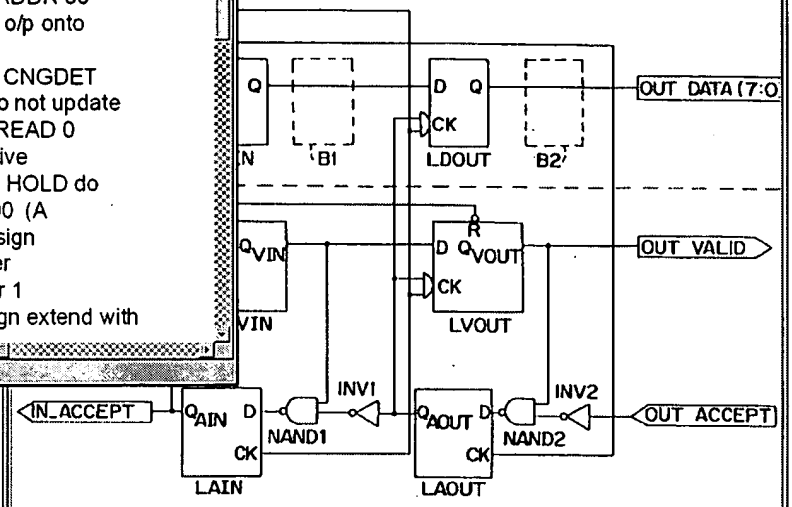


FIG. 4

	U	1	Document ID	Issue Date	
19			US 6353401 B1	20020305	Optical se
20			US 6263422 B1	20010717	Pipeline p response